Notice of Allowability	Application No.	Applicant(s)	
	09/593,945	NAOE, HITOSHI	
	Examiner	Art Unit	
	Jean B. Corrielus	2637	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *9/15/05*.

2. ☒ The allowed claim(s) is/are *1-15, renumbered as 1,2, 4, 5, 10, 6, 7, 14, 8, 11, 12, 9, 13, 15 and 3 respectively*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
   1. ☒ Certified copies of the priority documents have been received.
   2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
   3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
   1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☐ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☒ Examiner's Amendment/Comment
8. ☐ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

Jean B Corrielus
Primary Examiner
Art Unit: 2637 10-15-05

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Charles Gorenstein on 10/07/05.

The application has been amended as follows:

IN THE CLAIMS:

Claims 1-3, 5, 7, 8, 12-15 have been amended as follow:

--1 . (Currently Amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock, the polyphase clock generation circuit including a plurality of delay circuits connected in series and the first one of said plurality of delay circuits [delaying] receiving the input clock, wherein each of said plurality of delay circuits generates one of said plurality of clocks;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation

circuit with respect to the clock generated by the first delay circuit that [delays] receives the input clock; and

a clock selecting circuit to which a polyphase clock is inputted from the polyphase clock generation circuit and which selects an outputted polyphase clock based on a detection result from the detection circuit.

2. (Original) The bit synchronizing circuit of claim 1, wherein the [polyphase clock generation circuit is formed by connecting a] plurality of delay circuits [which] delay the input clock by almost the same amount of time.

3 . (Currently Amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock, the polyphase clock generation circuit including a plurality of delay circuits connected in series and the first one of said plurality of delay circuits receiving the input clock, wherein each of said plurality of delay circuits generates one of said plurality of clocks;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the clock generated by the delay circuit that delays the input clock;

a logic circuit to which an output from the detection circuit is inputted; and

a latch circuit to which an output from the logic circuit is inputted and of which an output is inputted to the logic circuit.

5. (Currently Amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock, the polyphase clock generation circuit including a plurality of delay circuits connected in series and the first one of said plurality of delay circuits [delaying] receiving the input clock, wherein each of said plurality of delay circuits generates one of said plurality of clocks;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the clock generated by the first delay circuit that [delays] receives the input clock ; and

an operational circuit for sampling an output from the detection circuit a plurality of times to generate a plurality of sampled values to carrying out an operation on the plurality of sampled values.

8 . (Currently Amended) A bit synchronizing circuit used for a reception circuit for serial communication, comprising:

a polyphase clock generation circuit for generating a plurality of clocks which are out of phase with each other by a regular interval, based on an input clock, the polyphase clock generation circuit including a plurality of delay circuits connected in series and the first one of said plurality of delay circuits [delaying] receiving the input clock, wherein each of said plurality of delay circuits generates one of said plurality of clocks;

a detection circuit for detecting which clock has a phase shift of an integral multiple of a clock cycle among the clocks generated by the polyphase clock generation circuit with respect to the clock generated by the first delay circuit that [delays] receives the input clock;

a plurality of bit synchronous working circuits to which a polyphase clock is inputted from the polyphase clock generation circuit so that a bit synchronizing operation is carried out at each different phase; and

a selecting circuit for selecting outputs from the plurality of bit synchronous working circuits, based on the detection result of the detection circuit.

12. (Original) The bit synchronizing circuit of claim 3, wherein the [polyphase clock generation circuit is formed by connecting a] plurality of delay circuits [which] delay the input clock by almost the same amount of time.

13. (Original) The bit synchronizing circuit of claim 5, wherein the [polyphase clock generation circuit is formed by connecting a] plurality of delay circuits [which] delay the input clock by almost the same amount of time.

14. (Original) The bit synchronizing circuit of claim 8, wherein the [polyphase clock generation circuit is formed by connecting a] plurality of delay circuits [which] delay the input clock by almost the same amount of time.

15. (Previously Amended) The bit synchronization circuit of claim 1, wherein said detection circuit comprises a plurality of flip-flops, each flip-flop having an input for said [one of said plurality of generated clocks] clock generated by said first delay circuit and an input for a respective clock among the clocks generated by the [polyphase clock generation circuit] the remaining delay circuits.--

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jean B. Corrielus whose telephone number is 571-272-3020. The examiner can normally be reached on Maxi-Flex.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jay Patel can be reached on 571-272-2988. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Jean B Corrielus
Primary Examiner
Art Unit 2637 10-15-05